Cadence SKILL and PCELL training course

23 - 25 October Cadence Location: Xilinx, City West, Dublin

This course is intended for IC physical layout engineers or mixed signal IC designers who also do IC layout. The course is divided into two days for SKILL and one day for PCELL training, with specific modules chosen from longer courses on each topic.

Prerequisites: SKILL: Experience accessing files and using a text editor in a Linux/UNIX environment. PCELL: Hands-on experience with Cadence Design Framework II and the Virtuoso Layout Editor is required. Familiarity with the SKILL Programming Language, being comfortable with UNIX/Linux and have a good working knowledge of at least one text editor.

Tuesday 23rd – Wednesday 24th October: SKILL Programming

Module 3 SKILL Programming Fundamentals
Lab 3-1 Using the Command Interpreter Window
Lab 3-2 Exploring SKILL Numeric Data Types
Lab 3-3 Exploring SKILL Variables
Lab 3-4 Displaying Data in the CIW
Lab 3-5 Solving Common Input Errors
Module 4 Working with Lists
Lab 4-1 Creating New Lists
Lab 4-2 Extracting Items from Lists
Module 5 Windows and Bindkeys Fundamentals
Lab 5-1 Opening Windows
Lab 5-2 Resizing Windows
Lab 5-3 Storing and Retrieving Bindkeys
Lab 5-4 Defining a Show File Bindkey
Module 6 Database Queries
Lab 6-1 Querying Design Databases
Module 9 Advanced Customization
Lab 18-1 Adding a Menu Item to the Schematic Edit Window
Lab 18-2 Adding a Pull-Down Menu to a Schematic Editor Window
Lab 18-3 Reversing the Layout Editor Pull-Down Menus
Lab 18-4 Customizing the Initial Window Placement
Module 10 SKILL Functions
Lab 9-1 Developing a SKILL Function
Module 11 The SKILL Interactive Development Environment (IDE)
Lab 10-1 Debugging a SKILL Program
Module 12 Flow of Control
Lab 11-1 Writing a Database Report Program
Lab 11-2 Exploring Flow of Control

Lab 11-3 More Flow of Control
Lab 11-4 Controlling Complex Flow

Thursday 25th October: SKILL Development of Parameterized Cells (PCells)

Module 1 Introduction to Parameterized Cells
Module 2 Using Relative Object Design Commands to Create Design Data
Lab 3-1 Creating Aligned Rectangles
Lab 3-2 Using ROD in a SKILL Procedure
Lab 3-3 Using ROD to Create a Cell
Lab 3-4 Creating ROD Objects Interactively
Lab 3-5 Investigating ROD Object Structure
Lab 3-6 Creating ROD Objects from Other ROD Objects
Module 3 Creating and Using SKILL Parameterized Cells
Lab 4-1 Creating a Simple SKILL PCell
Lab 4-2 Creating an Elementary Transistor Structure
Lab 4-3 Adding Source and Drain Connections Using Multipart Paths
Lab 4-4 Multipart Path Transistor (Optional)
Lab 4-5 Experimenting with Process Independence (Optional)
Enhanced Capabilities of SKILL PCells
Lab 6-1 Creating PCell Hierarchy
Lab 6-2 Using ROD Points in Hierarchy
Lab 6-3 Adding a CDF Parameter to the Inverter Cell
Lab 6-4 Using Autoabutment for the Virtuoso Layout Suite XL