DRAFT – 30 July 2021

SAR ADC Design Workshop

This highly interactive SAR ADC design workshop will take participants through the design of a 10-bit Successive Approximation (SAR) ADC on a low cost 0.18 um 1.8 V CMOS process using switched capacitor techniques. It will consist of a blend of learning approaches including concept and theory lectures, hands-on circuit design and lab simulation sessions, quizzes, Q&A, and demonstrations. A digital credential (badge) will be awarded on completion. The tutor for this workshop is Ken Deevy. Ken recently delivered a 12-week online CPD module in Analog IC Design to 20 engineers from Midas member companies.

The workshop is ideal for junior analog/mixed-signal design engineers but will also meet the needs of more experienced engineers in other roles, for example digital system design engineers, verification engineers, physical design engineers, test engineers. By the end of the workshop each participant will have gone through the process of modelling, building, and simulating a fully functioning CMOS 10-bit switched capacitor successive approximation A/D converter. The workshop will be delivered on 5 half days over a 2-week period. Online support will be provided to facilitate participants to complete any lab exercises during the workshop and for up to 4 weeks afterwards.

Workshop Overview

DAY 1 (09.00 to 13.00)
Concepts: Data converter fundamentals, MOS switch characteristics, switch errors, D/A settling time, data converter performance specifications, SAR ADC algorithm.
Labs: Voltage Mode DAC, D/A behavioural model, Comparator behavioural model

DAY 2 (09.00 to 13.00)
Concepts: SAR logic design, MOS capacitors and switches, charge injection and clock feedthrough, behavioural SAR ADC design & simulation.
Labs: Switch charge injection and clock feedthrough, behavioural SAR ADC.

DAY 3 (09.00 to 13.00)
Concepts: Dynamic circuits, sampling circuits, reduction of charge-injection & clock feedthrough, charge redistribution, switched capacitor(SC) DAC, settling time, split array technique, kT/C noise.
Labs: Charge redistribution, SAR control logic, 10-bit split-array behavioural model.

DAY 4 (09.00 to 13.00)
Concepts: SC SAR ADC signal sequence analysis, charge-injection & clock feedthrough considerations, differential topology, parasitic capacitance, capacitor orientation, bottom plate sampling.
Labs: 10-bit CMOS switched capacitor SAR ADC.

DAY 5 (09.00 to 13.00)
Concepts: Introduction to sampled data comparators, offset cancellation, introduction to digital calibration, other design considerations (reference settling, DFT, 1 V design, error budget).
Labs: 10-bit SAR ADC Test Bench, sampled-data comparator.

Key Learning Outcomes

- ✓ Interpret and evaluate data converter performance specifications
- ✓ Simulate and evaluate behavioural models for mixed signal circuits
- ✓ Simulate and evaluate CMOS switched capacitor circuits
- ✓ Design and simulate a SAR ADC behavioural model
- ✓ Evaluate and simulate a CMOS SAR ADC using switched capacitor techniques