Arm Cortex-M7 SoC Design online course (5 x 6 hour sessions)

Program Overview

This technical class will provide the required knowledge to support the hardware and firmware development of System on Chips based on the Arm Cortex-M7 micro-controller.

Learning Outcomes

By the end of this class the students will have an in-depth knowledge of the Cortex-M7 programmer's model including exception handling, memory management and micro-architectural details. In addition the students will acquire the knowledge related to integration tasks such as the processor's interfaces and bus protocols such as AXI, AHB, and APB.

Who is the course for?

This class will benefit ASIC design engineers as well as verification engineers who want to be able to integrate and develop test programs to validate the SoC logic surrounding the Arm Cortex-M7 macro-cell.

Course Outline

- **Cortex-M7 Overview**

  Block diagram • Architectural features • Instruction set • Programmer's model • Memory map • Memory interfaces • Caches • Exception handing • Memory protection • Power management • Implementation options

- **ARMv7-M Programmers' Model**

  Data types • Core registers • Modes, privileges and stack • Exceptions • Instruction set overview

- **ARMv7-M Assembly Programming**

  Data processing instructions • Load/Store instructions • Flow control • Miscellaneous instructions

- **Cortex-M7 Processor**

  Processor Pipeline • Execution Pipelines • Prefetch Unit • Memory-mapped Registers

- **Introduction to AMBA Protocols**

  AMBA APB • AMBA AHB • AMBA AXI

- **Cortex-M7 L1 Sub-Systems**

  Caches • Tightly coupled memory (TCM) • System considerations

- **ARMv7-M Exception Handling**

Exception Model • Interrupts • Writing the vector table and interrupt handlers • Internal exceptions and RTOS support • Fault exception

- **The SysTick Timer**

Programmer's Interface • Configuration Options

- **ARMv7-M Memory Model**

Memory address space • Memory types and attributes • Alignment and endianness • Barriers

- **ARMv7-M Memory Protection Unit**

Memory protection overview • Regions overview • Regions overlapping • Setting up the MPU

- **ARMv7-M Debug**

Coresight and debug access port DAP • Debug event and reset • Flash patch and breakpoint unit (FPB) • Data watch point and trace unit (DWT) • Instrumentation trace macrocell (ITM) • Embedded trace macrocell (ETM) • Trace port interface unit (TPIU) • Implementation details

- **ARMv7-M Extensions**

DSP • Floating Point

Trainer Profile

Dr David Cabanis is a principal engineer at Doulos, he is an Arm expert and holds Both the Arm Accredited Application Engineer and Arm Accredited Micro-controller Engineer certifications. He started his career in microelectronics at IBM in the UK and since then he has been a freelance consultant as part of Cadence ASIC design and verification team for 11 years. Having joined Doulos in 2009 David specialises in Arm training as well as system level modelling with SystemC/TLM and hardware design and verification with VHDL/SystemVerilog.