Aer Media Labs

ASIC/FPGA RTL Design Engineer

Background:

AerMediaLabs Ltd. is a recently formed fabless semiconductor company. We develop leading-edge wireless connectivity IP with an initial focus on developing the most advanced features for Bluetooth Low Energy. We have offices in Cork, Ireland and Bristol, UK.

Job summary:

We are seeking ASIC/FPGA RTL design and verification engineers to grow our team in Cork, with hybrid / home working a possibility. Working closely with the systems and software development teams, the role focuses on the hardware architecture, development, verification, and support of highest quality connectivity IP. This is an exciting opportunity for qualified engineers who have a passion for digital electronics and software development.

You will work directly on the IP development in collaboration with senior experts, so if you're looking for hardcore design, you've found it. We offer a very competitive remuneration package which includes pension, medical and life assurance, plus a stock option programme that we believe is unrivalled since Silicon Valley in the 90's.

Responsibilities and duties:

- Definition of digital CMOS ASIC subsystem architectures and test plans
- RTL implementation for optimal power, performance, area on leading-edge nodes
- Verification (test bench construct, debug, code coverage, regression testing)
- Mapping to FPGA in support of software development and system validation
- Documentation for internal and external purposes

Essential skills and experience:

- Proficient in VHDL (preferred), Verilog, and/or SystemVerilog
- Adept at rapidly understanding existing and new concepts and designs
- Proficient in implementation and debug of complex control/data path designs
- ASIC synthesis, constraint definition, formal and gate level verification/debug
- Ability to understand algorithms written in pseudo-code, C, C++, Matlab, etc.
- Ability to understand and develop scripts in; e.g. Python, Perl, TCL, UNIX shell script

Desirable skills and experience:

- Sound grasp of communication systems and digital signal processing techniques
- Understanding of bus fabric, processor, memory, and DMA subsystem architectures
- Implementation and verification of UPF power intent file
- Software/firmware development using Assembly, C, C++, or other languages
- Use of UVM metric driven verification mythology using SystemVerilog
- Familiarity with wireless standard specifications, particularly Bluetooth

Please submit CV with covering email to gary.wass@aermedialabs.com

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